In the Claims:

Please add new claims 6-10 as indicated below. This listing of claims replaces all prior versions.

1. (Previously Presented) A circuit comprising:

a plurality of interconnected logic blocks;

a main clock generator for distributing a reference clock signal to the logic blocks;

at least one local clock generator in each logic block for generating a respective set of synchronized local clock signals from the reference clock signal for further provision to respective elements of the logic block;

wherein a set of local clock signals of a first block is phase shifted relative to a set of local clock signals of a second block.

2. (Previously Presented) The circuit of claim 1, wherein the first and second blocks communicate via a one-way data path.

3. (Original) The circuit of claim 2, wherein the first block comprises a first logic cell configured to write data onto the one-way data path on a rising edge of one of the local clock signals of the first block provided at an enable input of the first logic cell and the second block comprises a second logic cell configured to read the written data from the one-way data path on a rising edge of one of the local clock signals of the second block provided at an enable input of the second logic cell.

4. (Original) The circuit of claim 2, wherein the first block comprises a first logic cell configured to write data onto the one-way data path on a rising edge of one of the local clock signals of the first block provided at an enable input of the first logic cell and the second block comprises a second logic cell configured to read the written data from the one-way data path on a falling edge of the reference clock signal provided at an enable

input of the second logic cell.

5. (Original) The circuit of claim 1, further comprising at least two additional blocks that communication via a two-way data bus and wherein respective sets of local clock signals of the at least two additional logic blocks are synchronized with each other.

6. (New) The circuit of claim 1, wherein the phase shift of the set of lock clock signals of the first block relative to the set of local clock signals of the second block reduces peak power consumption of the circuit.

7. (New) The circuit of claim 3, wherein the first and second logic cells are flip-flop cells.

8. (New) The circuit of claim 1, wherein the first block includes first and second flip-flop cells that are enabled by respective clock signals of the set of local clock signals of the first block and that each have a data input and a data output, the first block further including combinatorial cells that couple the data output of the first flip-flop cell to the data input of the second flip-flop cell.

9. (New) The circuit of claim 8, wherein the second block includes third, fourth and fifth flip-flop cells that are enabled by respective clock signals of the set of local clock signals of the second block and that each have a data input and a data output, the second block further including combinatorial cells that couple the data output of the third flip-flop cell to the data input of the fourth flip-flop cell, and wherein the data output of the second flip-flop cell is coupled to the data-input of the fifth flip-flop cell via a one-way data path.

10. (New) The circuit of claim 9, wherein the second block further includes a sixth flip-flop cell that is located on the one-way data path between the second and fifth flip-flop cells and that has a data input and a data output, the data input of the sixth flip-flop cell being coupled to the data output of the second flip-flop cell and the data output of the sixth flip-flop cell being coupled to the data-input of the fifth flip-flop cell.